Direct Time-of-Flight Sensor System Based on SPAD IC

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***Abstract*—In recent years, direct time-of-flight (dToF) sensor systems have become crucial in autonomous vehicles, light detection and ranging (LiDAR), and 3D imaging applications. Single-photon avalanche diodes (SPADs), highly-sensitive detectors capable of capturing individual photons, play a vital role in the systems by enabling high-resolution imaging and accurate distance measurement. Time-to-digital converters (TDCs) are crucial for dToF systems as they allow for high-precision, picosecond-level measurements by converting time intervals into digital values. In this paper, we present the design of TDC using a voltage-controlled Vernier delay line. We also show simulation results of the dToF system, which include the analog front-end (AFE) for the SPAD, TDC, and FPGA-based histogram, using a Verilog-A SPAD model based on SPAD's characteristics.**

Keywords—Direct time-of-flight (dToF), histogramming, light detection and ranging (LiDAR), single-photon avalanche diode (SPAD), time-to-digital converter (TDC), Vernier delay line.

I. Introduction

Direct time-of-flight (dToF) sensors are a key technology in many emerging applications such as autonomous driving, light detection and ranging (LiDAR) [1]-[6], robotics [7], and augmented reality (AR) [8], where accurate distance measurement and 3D imaging are essential. The core principle of dToF systems is to measure the time for a light pulse to travel to a target and return, enabling precise distance computation. A critical component in this process is the single-photon avalanche diode (SPAD), which can detect single photons due to its high sensitivity. SPADs are widely used as receivers in dToF and LiDAR systems, where accurate and high-resolution distance data is necessary [9], [10].

In dToF systems based on SPAD ICs, the design of the time-to-digital converter (TDC) is of utmost importance [11], as it must consider the unique characteristics of SPADs. SPADs have a specific noise characteristic known as dark count rate (DCR), where carriers trapped within the device can be released even without light, leading to false signals. The TDC's response to all such dark counts significantly impacts the accuracy of the measurements and power consumption, making its design a critical aspect of dToF systems. This paper proposes an optimized TDC for a dToF sensor system based on a SPAD, which processes SPAD signals only within specific time intervals, thereby reducing unnecessary power consumption. The architecture consists of a 6-bit asynchronous coarse counter TDC and a fine TDC using a voltage-controlled Vernier delay line [12]-[16]. The fine TDC enhances accuracy by correcting both the rising and falling edges of the distance measurement data provided by the coarse TDC. The delay line is also designed using D-flip flops with transmission gates to minimize gate delay and improve output results. The TDC implemented in a 90nm CIS process achieves a dynamic range of 64 times the reference clock period, with voltage-controlled precision ranging from 30ps to 50ps. We utilized a Verilog-A SPAD model that incorporated the effects of dark count rate (DCR) and avalanche behavior [17]-[18] to simulate the dToF system. This simulation included the analog front-end (AFE) for SPAD, TDC, and FPGA-based histograms. The purpose of this simulation was to validate the TDC's operation and performance in conditions that closely resemble those of an actual SPAD-based dToF system.

This paper will first introduce the architecture of the circuits comprising the dToF system in Section II, explain the principles of the voltage-controlled Vernier delay line TDC, and discuss the techniques used to reduce power consumption and improve accuracy. Section III presents the simulation results of the dToF system, while Section IV summarizes and concludes the work.

II. System Architecture

A. Analog front-end (AFE)

The SPAD operates in Geiger mode when a reverse bias greater than its breakdown voltage is applied, resulting in avalanche multiplication when a photon is detected. This produces a significant current, typically in the milliampere range, which generates an output pulse. The role of the AFE in the SPAD-based dToF system is to reduce the SPAD output's dead time from microseconds to tens or hundreds of nanoseconds, as shown in Fig. 1.

Reducing the dead time is crucial because it allows the system to detect a higher number of photons within a given time frame, increasing the overall temporal resolution and

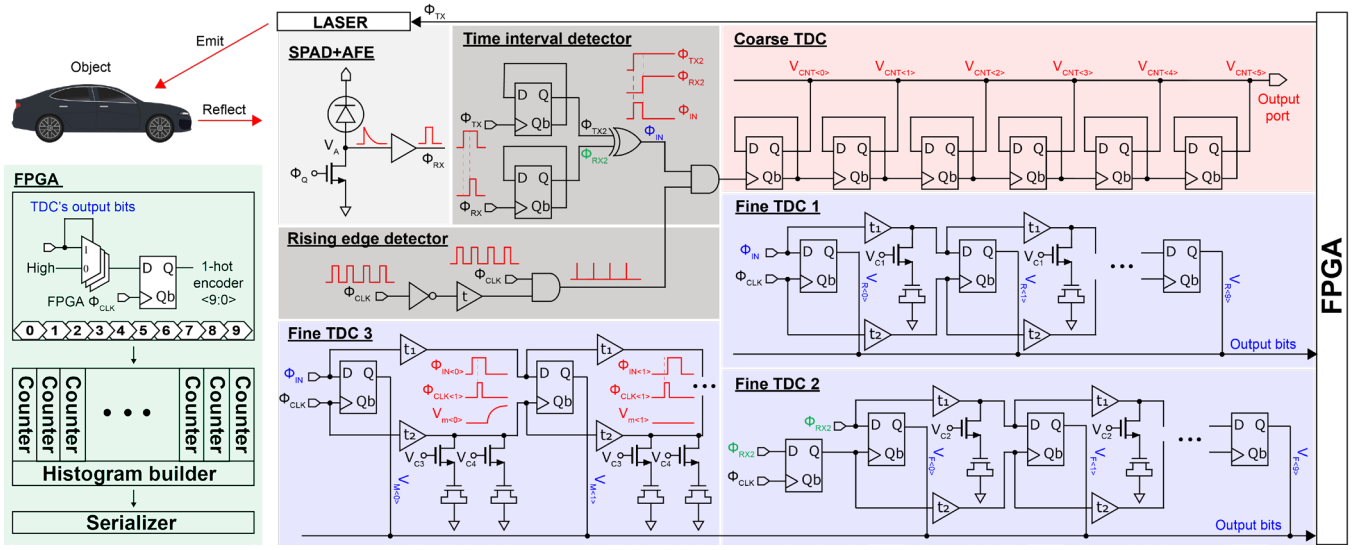

Fig. 1. Architecture of the dToF sensor system based on a SPAD IC.

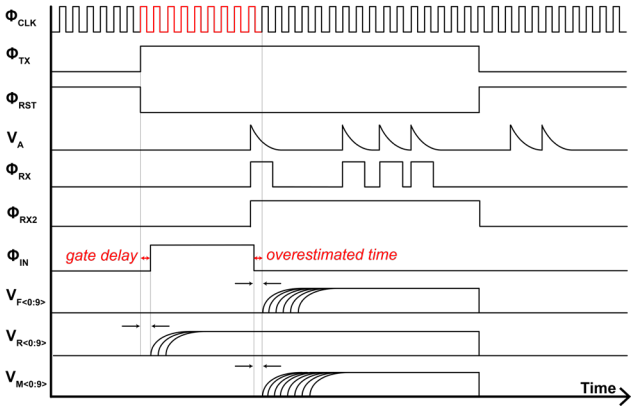

Fig. 2. Timing diagram of the dToF system showing reference clock (Φ_{CLK}), Φ_{TX}, reset clock (Φ_{RST}), SPAD detection (Φ_{RX}), time interval (ΦI_N), and fine TDC's outputs.

accuracy of the dToF system. The AFE achieves this by rapidly quenching the avalanche process and resetting the SPAD, preparing it for subsequent photon detection events. Furthermore, by conditioning the SPAD's output, the AFE ensures compatibility with downstream digital circuits such as the TDC and FPGA, facilitating precise time measurements and efficient data processing.

B. Time-to-digital converter (TDC)

In the dToF system illustrated in Fig. 1, the FPGA triggers the laser using a clock signal, Φ_{TX}, while the SPAD and AFE detect the returned signal, Φ_{RX}. The time interval (Φ_{IN}) between Φ_{TX} and Φ_{RX} is measured using a TDC synchronized with the reference clock, which starts with the Φ_{TX} signal, to compute the distance. This setup ensures that the timing of the laser pulse and the detection of the reflected signal are accurately captured, allowing for precise distance measurement.

The designed TDC comprises a 6-bit coarse counter and three fine TDCs based on a voltage-controlled Vernier delay line. The three fine TDCs include one with a 30ps resolution and two with a 40ps resolution, which measures the time intervals between the rising and falling edges of the Φ_{IN} signal and the reference clock to correct the time measurement and improve system accuracy. To manage the data effectively and reduce unnecessary power consumption, the system employs D-flip flops to store the Φ_{TX} and Φ_{RX} signals. This storage process is crucial in halting further inputs before the next Φ_{TX} signal arrives, thereby preventing the SPAD's false output made by DCR from being processed [19]. The time interval between the stored signals is then detected using the XOR gate, and the coarse TDC measures the time interval by counting the number of rising edges of the reference clock within the Φ_{IN} pulse width.

The fine TDC 1 and fine TDC 2, as shown in Fig. 1, play a crucial role in the system's precision. They measure the time between the rising edge of the Φ_{TX} signal and the rising edge of the Φ_{IN} signal, as well as the time between the falling edge of the Φ_{IN} signal and the rising edge of the next reference clock. These measurements are instrumental in correcting any delays introduced by gate delays in the D-flip flops and adjusting for any overestimated time from the coarse TDC, thereby ensuring the system's precision and accuracy. The timing diagram of the proposed dToF system is shown in Fig. 2. In addition to correcting both the rising and falling edges using the fine TDCs, the design incorporates two key techniques to enhance system accuracy. First, the fine TDCs use a voltage-controlled Vernier delay line to provide fine resolution adjustments, compensating for process variations in fabricated chips. This allows fine TDC 1 and fine TDC 2 to have a base resolution of 40ps, which can be adjustable to 50ps, while fine TDC 3, performing the same role, achieves a resolution of 30ps. Second, D-flip flops are implemented using transmission gates, which minimize gate delay and ensure more robust signal propagation, improving both timing accuracy and output precision.

C. FPGA-based histogram

In the proposed dToF system, the FPGA-based histogram processes real-time distance information, allowing for efficient data collection and analysis. The system first uses a 2-to-1 mux, where the select signal and input signal are connected to the 10-bit output of the TDC. A custom-designed one-hot encoder then detects the bit's position where the output transitions from 1 to 0, effectively encoding the TDC result [19]. This encoded data is fed into a histogram builder composed of ten 12-bit

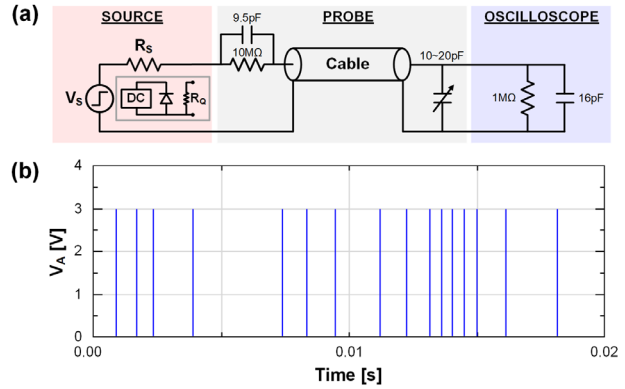

Fig. 3. (a) Verilog-A SPAD model simulation schematic with the equivalent circuit model of parasitic components in the measurement environment. (b) Simulation results of the Verilog-A SPAD model.

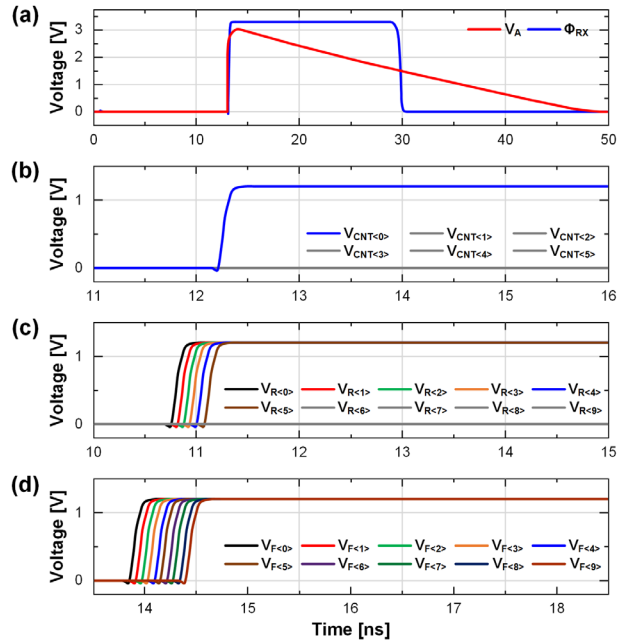

Fig. 4. Simulation results of AFE and TDC with time interval measurement and correction. (a) Simulated SPAD pulse and AFE output. (b) Coarse TDC measurement with reference clock. (c) Fine TDC output measuring gate delay between Φ_{TX} and Φ_{IN}. (d) Fine TDC output correcting the overestimated time interval measured by coarse TDC.

counters. Each counter corresponds to a specific distance range, and the histogram builder updates these counters in real time based on the distance information received. This real-time histogram construction enables the system to visualize and analyze the distribution of distance measurements over time.

III. Simulation Results

The Verilog-A SPAD model, which accurately reflects the SPAD's characteristics—including dark count rate (DCR) and avalanche behavior—was used to simulate the dToF system circuits. To simulate realistic measurement conditions, we incorporated the parasitic components of probes and oscilloscopes into an equivalent circuit within the Verilog-A SPAD model. This approach provided a more accurate simulation, closely mimicking actual hardware behavior. Fig. 3 shows the Verilog-A simulation results, demonstrating that the DCR characteristics were well reflected in the model. This validates the proposed

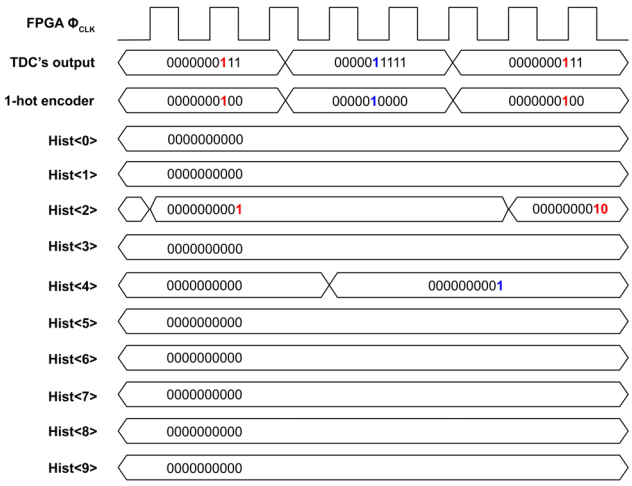

Fig. 5. Simulation results of FPGA-based histogram.

TDC's robustness in handling SPAD behavior, including the effects of DCR, and ensures the system's overall accuracy.

In Fig. 4(a), the simulation results of the AFE and TDC, conducted in the Virtuoso environment, are presented. The time interval between Φ_{TX} and Φ_{RX} used in the simulation is 2.56ns, corresponding to a distance of 37.76cm. The reference clock used has a frequency of 625MHz, corresponding to a period of 1.6ns. Due to gate delays, the time interval Φ_{IN} between Φ_{TX} and Φ_{RX} has a delay, causing the system to miss counting the first reference clock synchronized with Φ_{TX}. As shown in Fig. 4(b), this causes the coarse TDC to output a value of 1. To address this, 1 is added to the coarse TDC value, and the overall time interval is corrected using fine TDCs. Fig. 4(c) shows the result of the fine TDC that measures the gate delay between the rising edges of Φ_{TX} and Φ_{IN}. The output changes from 1 at the 6th bit to 0 at the 7th bit, indicating that the measured time interval is between 6 and 7 cycles of the fine TDC's 40ps resolution, equating to approximately 240ps to 280ps. In Fig. 4(d), the fine TDC measures the time interval between the falling edge of Φ_{IN} and the next rising edge of the reference clock. All ten output bits are set to 1, indicating that the time interval measured is between 400ps and 440ps. This compensates for the overestimation by the coarse TDC. Using these simulation results, we can calculate the total time interval as:

$$(coarse\ TDC+1) \times 1.6ns - (Fine\ TDCs)$$
$$= 2 \times 1.6ns - 16 \times 40ps = 2.56ns \quad (1)$$

which confirms the accuracy of the distance measurement.

Fig. 5 illustrates how the 10-bit outputs of the fine TDCs are histogrammed in real-time by the FPGA's 50MHz clock [20], [21]. The simulation results show that the system successfully processes the time intervals and constructs a histogram for real-time distance information.

IV. Conclusion

We present an optimized TDC for a dToF sensor system based on a SPAD, fabricated using a 90nm CIS process. The microphotograph of the TDC chip is shown in Fig. 6. The TDC chip comprises a coarse TDC, fine TDC with adjustable fine resolution via voltage control, and a

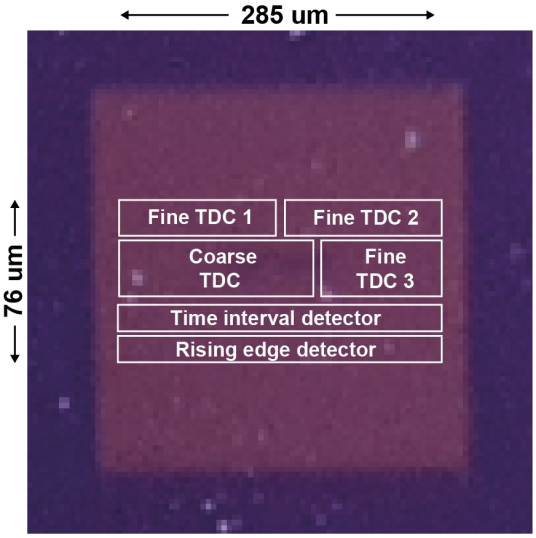

Fig. 6. Microphotograph of the TDC chip fabricated in a 90nm CIS process.

detector that captures the rising edge of the reference clock and measures the time interval between Φ_{TX} and Φ_{RX}. The output accuracy was significantly improved by utilizing D-flip flops designed with transmission gates. The system ensures that only one Φ_{RX} signal is processed per Φ_{TX} clock cycle, effectively reducing unnecessary power consumption caused by SPAD's false outputs.

Furthermore, we simulated the dToF system circuit using the optimized TDC with a Verilog-A SPAD model that accurately reflects the SPAD's operating characteristics, including DCR and avalanche behavior. This allowed us to verify the operation of the TDC in a realistic environment, similar to how it would function with an actual SPAD in the dToF system. We conducted simulations with a time interval of 2.56ns, corresponding to a measured distance of 37.76 cm. The results confirmed the accuracy of the TDC's time interval measurements, demonstrating the reliability of the design in precise distance measurements.

This work successfully demonstrates an efficient approach to time measurement in SPAD-based dToF systems, reducing power consumption and enhancing accuracy. The design approach, including techniques for fine resolution adjustment and gate delay minimization, along with the simulation results, paves the way for further improvements in high-precision distance measurement systems for various applications such as LiDAR and 3D imaging.

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